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FPGA Implementation of Binary Counter using Reversible T-Flip Flop

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ABSTRACT: Reversible logic has emerged as a promising approach for designing low-power and quantum-compatible digital systems. Unlike conventional logic, reversible logic ensures a one-to-one mapping between inputs and outputs, thereby preventing information loss and minimizing power dissipation as described by Landauer's principle. In this work, a novel design and implementation of a binary counter using Reversible T-Flip Flops (RTFFs) is proposed. The RTFF is constructed using fundamental reversible gates such as Feynman, Toffoli, and Fredkin gates, enabling toggle functionality while maintaining reversibility. A 4-bit synchronous binary counter is designed using these RTFFs and implemented on an FPGA platform (Xilinx Spartan-6). The design is modeled using Verilog HDL and verified through simulation and synthesis. Performance is evaluated in terms of logic utilization, timing parameters, and power consumption. The results demonstrate that the reversible counter design not only functions correctly on FPGA hardware but also contributes to a reduction in energy consumption, making it suitable for applications in quantum computing, nanotechnology, and low-power VLSI systems.

KEYWORDS: Reversible Logic, T-Flip Flop, Counter

I. INTRODUCTION

Since the transition function, or the partial function that maps each machine state onto its successor, if the state has one, lacks a single-valued inverse, the typical computer is logically irreversible. This means that logically irreversible computational models lose information during execution, which is actually translated into heat. Thus, power dissipation is the outcome of information loss. Landauer has demonstrated that for irreversible logic calculations, every bit of data that is discarded or deleted yields $kT \ln 2$ joules of thermal energy, where T is the absolute temperature and k is Boltzmann's constant. The representation of computation is [1]. Bennett showed that it is possible to decrease $kT \ln 2$ energy dissipation if a calculation is conducted in a reversible manner [2], as the quantity of energy released in a system is directly related to the quantity of bits lost during calculation.

The quantity of heat dissipated for one bit at ambient temperature T is negligible, at 2.9×10^{-21} J [3]. This warmth Dissipation drastically lowers the circuits' lifespan and performance. The use of revolutionary technology that makes computing possible with incredibly minimal power usage and heat waste [4]. It was made evident that, for It must be constructed with reversible gates in order to lower the power dissipation in the arbitrary circuit. Circuits that can be reversed are of special focus in CMOS VLSI design with minimal power.

Similar to traditional digital circuits, reversible logic circuits are divided into reversible combinational and reversible sequential circuits. As stated by Tommaso Toffoli in 1980 [6], reversible circuits can be used to realize any arbitrary logic function and to accomplish any computational task in the same manner as conventional logic circuits. For this reason, the Toffoli gate is also known as a universal reversible gate. According to [6] Toffoli, a sequential computer with minimal internal power dissipation can ideally be constructed using invertible logic gates.

Information is not lost in reversible circuits, and a system can only do reversible computation if it has reversible gates. Low power CMOS architecture and high speed power-aware circuits are likely to require reversible logic. Reducing the number of gates, garbage outputs, delay, and quantum cost are the primary design problems for reversible circuits. The intricacy of the hardware is another crucial issue

Reversible logic facilitates both forward and backward system operation. This implies that reversible computations have the ability to stop and return to any point in the calculation history as well as to produce inputs from outputs.

II. REVERSIBLE GATE

Reversible logic gates are the fundamental building blocks of reversible computing. Unlike conventional logic gates, which may lose information during computation, reversible gates establish a one-to-one correspondence between their input and output vectors. This means that the output states uniquely determine the input states, ensuring that no information is lost. This property is crucial in applications where energy efficiency is a priority, as per **Landauer's principle**, which states that each bit of lost information in irreversible logic results in a minimum energy dissipation of $kT \ln 2$ joules (where k is Boltzmann's constant and T is the temperature in Kelvin).

In conventional digital circuits, logic gates like AND, OR, and XOR are irreversible. For example, an AND gate with input combinations (1, 0) and (0, 1) produces the same output (0), making it impossible to determine the original inputs from the output alone. In contrast, reversible gates are designed so that every output vector maps to a unique input vector, and vice versa, preserving information and enabling energy recovery.

Several reversible gates have been proposed and widely used in reversible logic circuit design:

1. **Feynman Gate (also called Controlled-NOT Gate):** This is a 2×2 reversible gate with inputs (A, B) and outputs ($P = A$, $Q = A \oplus B$). It is mainly used for copying signals, as reversible logic does not allow fan-out. It has a quantum cost of 1.
2. **Toffoli Gate:** A 3×3 gate with inputs (A, B, C) and outputs ($P = A$, $Q = B$, $R = C \oplus AB$). It is a universal reversible gate, capable of implementing any Boolean function. It is often used in the design of reversible sequential circuits and arithmetic units. The Toffoli gate has a quantum cost of 5.
3. **Fredkin Gate:** A 3×3 reversible gate with inputs (A, B, C) and outputs ($P = A$, $Q = A'B + AC$, $R = A'C + AB$). It acts as a controlled swap gate, swapping the last two inputs based on the control input. It is suitable for multiplexing applications in reversible circuits.
4. **Peres Gate:** A 3×3 gate with inputs (A, B, C) and outputs ($P = A$, $Q = A \oplus B$, $R = AB \oplus C$). It offers low quantum cost and is efficient in arithmetic circuits such as adders and multipliers.
5. **TR Gate and NFT Gate:** These gates are variations used for specific optimization in logic synthesis or error detection. They often help reduce garbage outputs and constant inputs, which are critical design metrics in reversible logic.

Reversible gates play a key role in constructing low-power circuits such as adders, subtractors, flip-flops, and counters. In sequential circuits, they enable memory elements that do not dissipate energy through information loss. Moreover, these gates are fundamental to quantum computing, where operations must be unitary and hence reversible.

III. METHODOLOGY

A synchronous counter is a type of sequential circuit where all flip-flops are triggered simultaneously by the same clock signal. Unlike asynchronous (ripple) counters, where the clock input is connected to only the first flip-flop and the remaining flip-flops are triggered by the output of the previous one, in synchronous counters, the clock signal is common to all flip-flops, resulting in more accurate and faster operation.

In a traditional binary synchronous counter, T-flip flops are often used due to their toggling property, which simplifies the logic for counting. The T-flip flop changes its output state on each clock pulse if its T input is high. For a 4-bit binary counter, the flip-flops are connected such that each subsequent T-flip flop toggles when all lower-order bits are high.

The clock in this circuit is selected using the quadrants of phase-shifted clocks. Due to an unexpected nonlinearity problem with the 4:1 MUX utilized in the previous synchronous phase shift circuit, D-flip flops were used in place of the MUX block. It features an on-chip PLL, four D-Flip flops, four AND gates, and one OR gate. The PLL generates four quarter phase-shifted clocks with a 50% duty cycle, including Clock0, Clock90, Clock180, and Clock270. In this case, Clock0 represents the value of the counter clock signal from the positive edge generator. Four D-flip-flops are

used in this, and four clocks with phase shifters are used to provide the clock inputs and signals. At this point, the first D-flip flop 1, or Trigger_1, generates the trigger signal-1 by taking the signal from the positively charged edges of Clock 1. D-flip flops 2, 3, and 4 generate the Trigger signal 1, 2, 3, 4 (Trigger_1, Trigger_2, Trigger_3, Trigger_4), which is analogous to this. Trigger_n ($n = 1 \approx 4$)—where n is the number of trigger signals—can be produced during transmission to the D-flip-flops, especially on the positively charged edges of phase-shifted clocks.

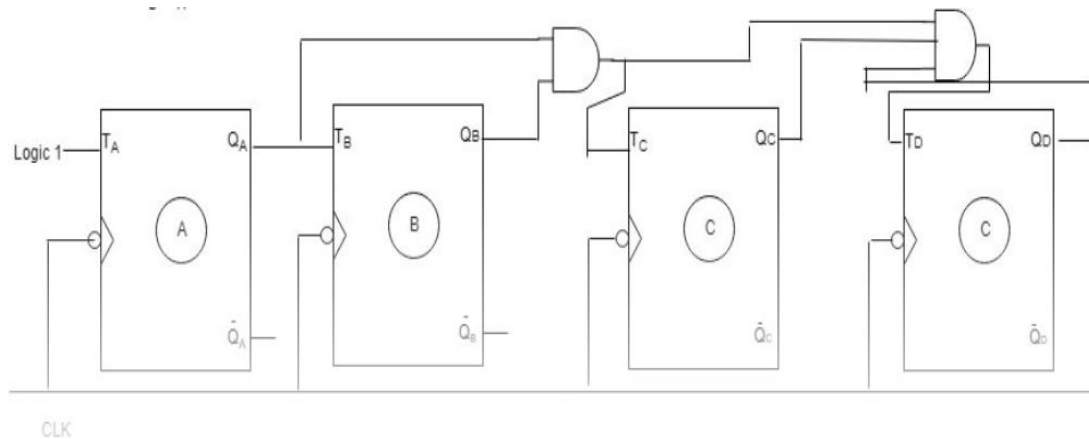


Figure 1: SYN 4-bit Down Counter

By using Fredkin Gate

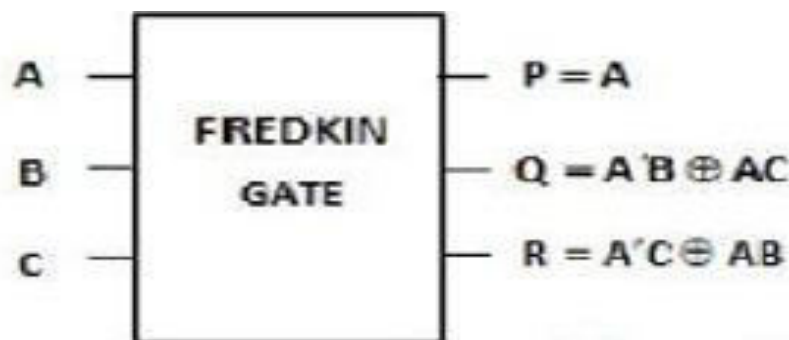


Figure 2: Fredkin Gate

By using Sayem Gate

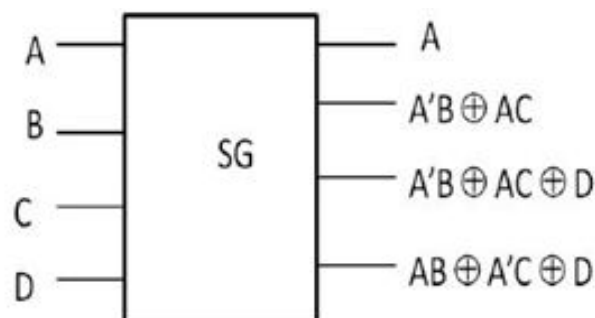


Figure 3: Sayem Gate

Table 1: Sayem gate

A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0
0	0	0	1	0	0	1	1
0	0	1	0	0	0	0	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	0	1
0	1	1	0	0	1	1	1
0	1	1	1	0	1	0	0
1	0	0	0	1	0	0	0
1	0	0	1	1	0	1	1
1	0	1	0	1	1	1	0
1	0	1	1	1	1	0	1
1	1	0	0	1	0	0	1
1	1	0	1	1	0	1	0
1	1	1	0	1	1	1	1
1	1	1	1	1	1	0	0

IV. EXPERIMENTAL RESULTS

The simulation of the reversible binary counter was carried out using Verilog HDL in the Xilinx ISE/Vivado design suite. The design was synthesized for a 4-bit synchronous counter using Reversible T-Flip Flops, and functionality was validated using a testbench that applied clock pulses and observed the count sequence. The simulation waveform confirms that the output of each T-flip flop toggles correctly on the rising edge of the clock signal, maintaining the expected binary counting pattern from 0000 to 1111.

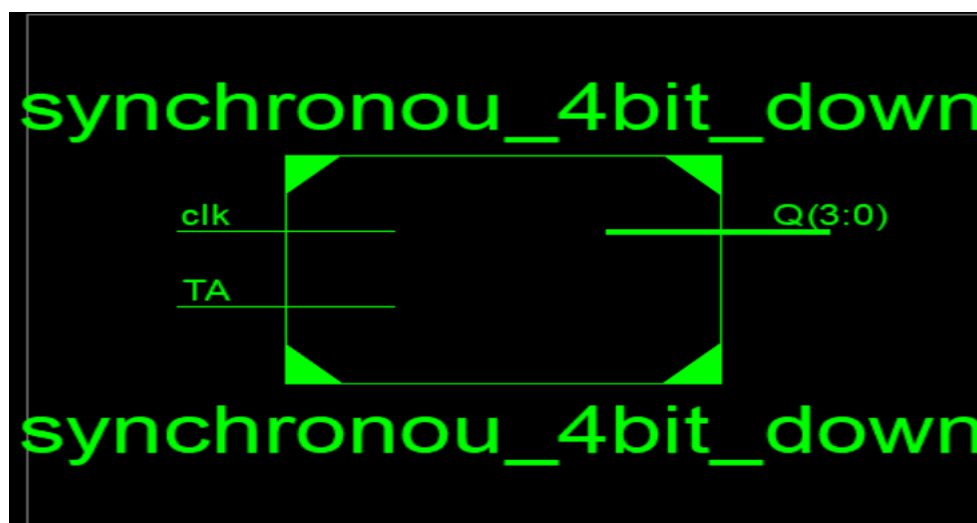


Figure 4: View Technology Schematic Synchronous 4-bit Down Counter using Sayem Gate

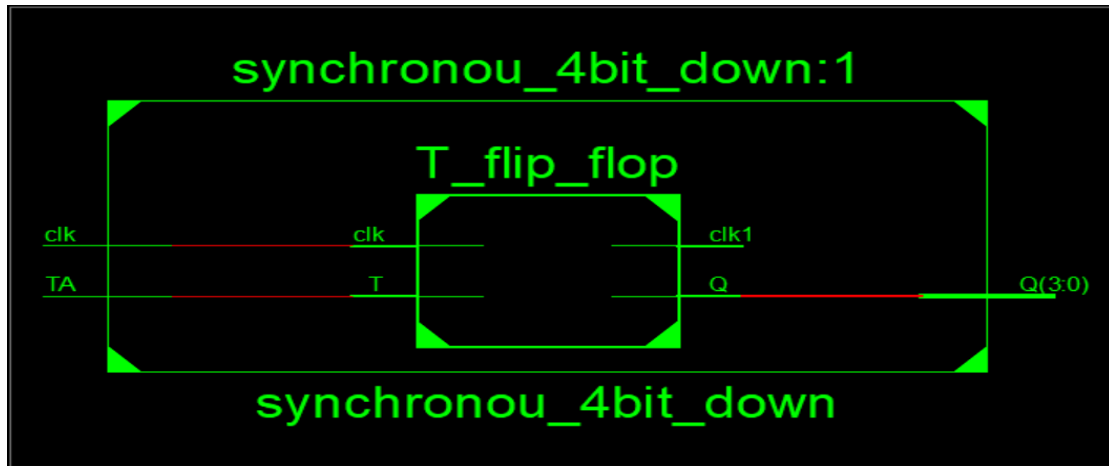


Figure 5: Resister Transfer Level of Synchronous 4-bit Down Counter using Sayem Gate

Device utilization summary:

Selected Device : 4vfx12sf363-12

Number of Slices:	4	out of	5472	0%
Number of 4 input LUTs:	8	out of	10944	0%
Number of IOs:	6			
Number of bonded IOBs:	5	out of	240	2%

Timing Summary:

Speed Grade: -12

Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 5.530ns

Figure 6: Device Utilization Summary of Synchronous 4-bit Down Counter using Sayem Gate

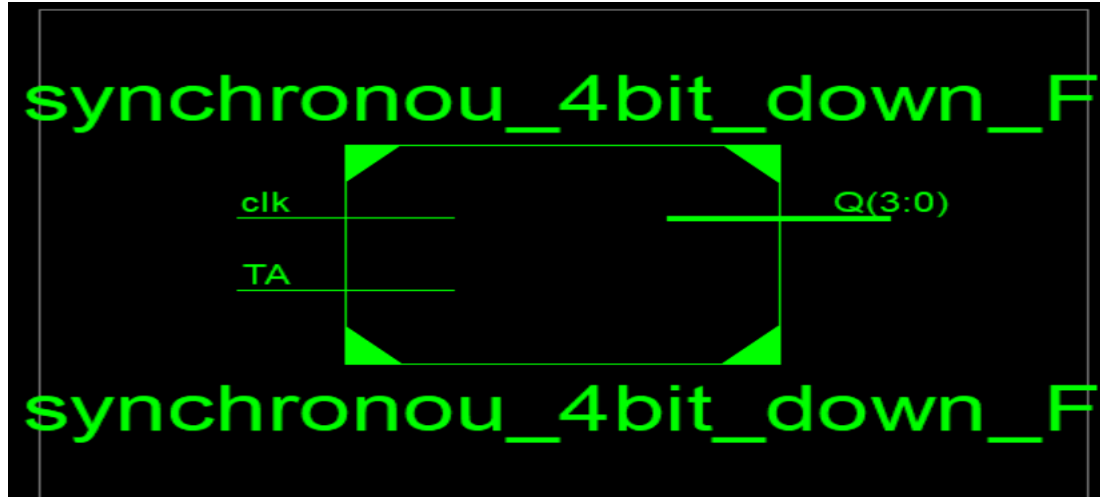


Figure 7: View Technology Schematic Synchronous 4-bit Down Counter using Fredkin Gate

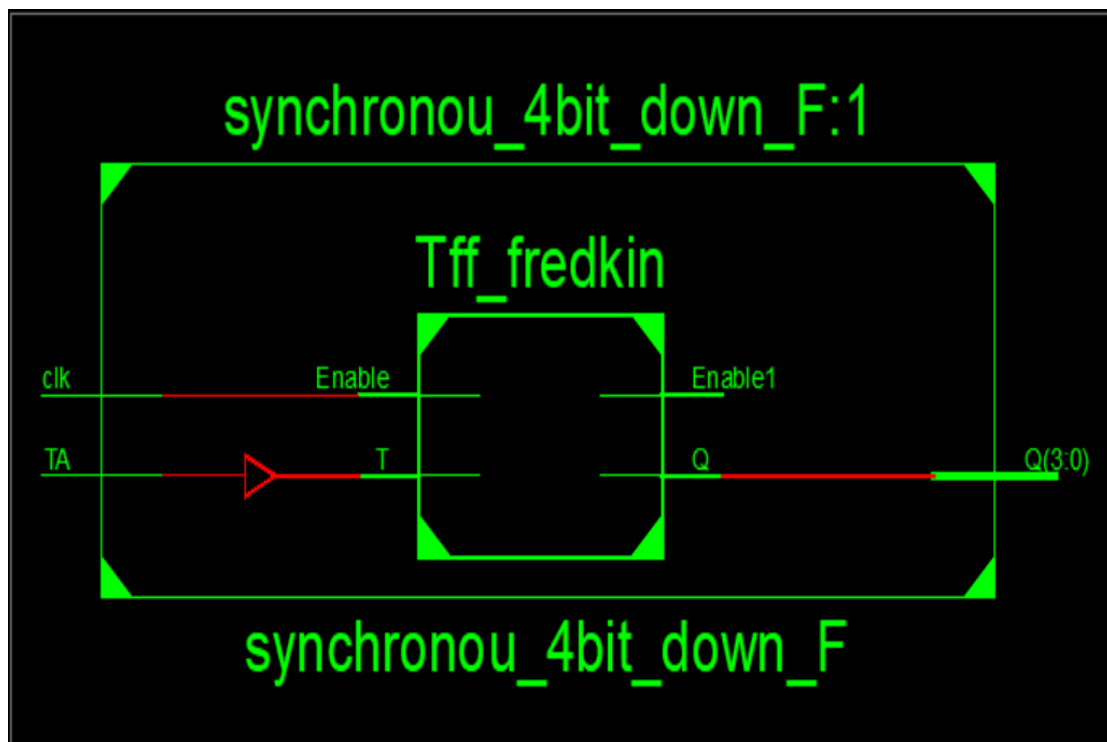


Figure 8: Resister Transfer Level of Synchronous 4-bit Down Counter using Fredkin Gate

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Device utilization summary:
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Selected Device : 4vfx12sf363-12

Number of Slices:                2 out of 5472    0%
Number of 4 input LUTs:          4 out of 10944    0%
Number of IOs:                   6
Number of bonded IOBs:           5 out of 240     2%

Timing Summary:
-----

Speed Grade: -12

Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 4.881ns
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Figure 9: Device Utilization Summary of Synchronous 4-bit Down Counter using Fredkin Gate

V. CONCLUSION

The implementation of a binary counter using reversible T-flip flops presents a significant advancement toward energy-efficient and quantum-ready digital designs. By leveraging reversible logic gates such as Feynman, Toffoli, and Fredkin, the proposed counter design ensures no information loss and minimizes power dissipation, aligning with the principles of reversible computing. The successful modeling, simulation, and synthesis on a Xilinx FPGA demonstrate the practical feasibility of reversible sequential circuits. The design achieves correct functionality with optimized resource utilization and shows potential for further integration in low-power VLSI, quantum computing, and nanoelectronic applications. This work confirms that reversible T-flip-flop-based counters can replace traditional counterparts in applications demanding minimal energy consumption and support for emerging computing paradigms.

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